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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,163	04/23/2001	Yoshio Oowaki	HITA.0050	4876

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2677	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,163	OOWAKI ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-12,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-12,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 7-12, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (US Patent No. 6, 462, 727 B2) in view of Takahara et al. (JP No. 04-168417) and Kim et al. (US Patent No. 6,067,063).

As to claim 7, Shin teaches a liquid crystal display device, comprising: a liquid crystal display element with plurality of drain signal (data) lines (See Figs. 2, 7, items 15, 24, Col. 1, Lines 36-45), a plurality of driving circuits including at least one odd numbered driving circuit and at least one even numbered driving circuit, each of the driving circuits having a plurality of output terminals (See Fig 7, items 240, 250, 270, 280, 290, Col. 5, Lines 28-53); a display control device transmitting display data alternately to one of the output terminals of odd numbered driving circuit and to one of the output terminals of even numbered driving circuit which is arranged next to the first driving circuit (See Fig. 7, items 200, 220, Col. 5, Lines 28-53), wherein the display control device has a first storing means for storing display data for odd numbered driving circuit (See Fig. 7, item 230a, Col. 5, Line 45) which are inputted externally (See Fig. 7, items C, D) and a second storing means for storing display data for even numbered driving circuit (See Fig. 7, item 230b, Col. 5, Line 49) which are inputted

externally (See Fig. 7, items C, D), wherein the display control device reads out the display data from the first storing means and second storing means alternately to transmit to plurality output terminals being connected to one of the drain signal lines through plurality of the driving circuits (See Figs. 7-8, items 230a-230b, 240, 250, from Col. 5, line 54 to Col. 6, line 17); wherein before transmitting a display datum to output terminal to the drain signal lines, the display control devices reads out from one of the first and second storing means a display datum and then repeatedly transmits display datum to all connected and not connected (all) to the drain signal lines (See Figs. 7-8, items 230a-230b, 240, 250, from Col. 5, line 54 to Col. 6, line 17).

Shin does not teach at least one of numbered driving circuits has at least one output terminal not being connected to the drain signal lines and each of the remaining output terminal being connected to one of the drain signal lines.

Takahara et al. teaches at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines (See Drawing 2, item 25) and to skip unconnected pins by generating start pulses for each IC with clock pulses (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Takahara et al. into Shin system in order to use the same driving circuit for a LCD panel when the output bit number of a driver IC is larger than the circuit number of the divided electrode groups (See from page 2, last line to page 3, line 3 in Takahara et al).

Shin and Takahara et al. do not teach scheduled to receive display datum immediately prior or subsequently to the transmitting of datum to output terminal being not connected to the drain signal lines.

Kim et al. teaches the display control device transmits to output terminal signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines (See Fig. 5, items Vi, Ui, Col.5, Lines 26-39).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Kim et al. into Takahara et al. and Shin system in order to improve the viewing characteristics of LCD (See Col. 2, Lines 38-40 in Kim et al. reference).

As to claim 10, Shin teaches a display device, comprising: a display element with plurality of drain signal (data) lines (See Figs. 2, 7, items 15, 24, Col. 1, Lines 36-45), a plurality of driving circuits including at least one odd numbered driving circuit and at least one even numbered driving circuit, each of the driving circuits having a plurality of output terminals (See Fig 7, items 240, 250, 270, 280, 290, Col. 5, Lines 28-53); a display control device transmitting display data alternately to one of the output terminals of odd numbered driving circuit and to one of the output terminals of even numbered driving circuit which is arranged next to the first driving circuit (See Fig. 7, items 200, 220, Col. 5, Lines 28-53), wherein the display control device has a first storing means for storing display data for odd numbered driving circuit (See Fig. 7, item 230a, Col. 5, Line 45) which are inputted externally (See Fig. 7, items C, D) and a second storing

means for storing display data for even numbered driving circuit (See Fig. 7, item 230b, Col. 5, Line 49) which are inputted externally (See Fig. 7, items C, D), wherein the display control device reads out the display data from the first storing means and second storing means alternately to transmit to plurality output terminals being connected to one of the drain signal lines through plurality of the driving circuits (See Figs. 7-8, items 230a-230b, 240, 250, from Col. 5, line 54 to Col. 6, line 17); wherein before transmitting a display datum to output terminal to the drain signal lines, the display control devices reads out from one of the first and second storing means a display datum and then repeatedly transmits display datum to all connected and not connected (all) to the drain signal lines (See Figs. 7-8, items 230a-230b, 240, 250, from Col. 5, line 54 to Col. 6, line 17).

Shin does not teach at least one of numbered driving circuits has at least one output terminal not being connected to the drain signal lines and each of the remaining output terminal being connected to one of the drain signal lines.

Takahara et al. teaches at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines (See Drawing 2, item 25) and to skip unconnected pins by generating start pulses for each IC with clock pulses (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Takahara et al. into Shin system in order to use the same driving circuit for a LCD panel when the output bit number of a driver IC is larger

than the circuit number of the divided electrode groups (See from page 2, last line to page 3, line 3 in Takahara et al).

Shin and Takahara et al. do not teach scheduled to receive display datum immediately prior or subsequently to the transmitting of datum to output terminal being not connected to the drain signal lines.

Kim et al. teaches the display control device transmits to output terminal signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines (See Fig. 5, items Vi, Ui, Col.5, Lines 26-39).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Kim et al. into Takahara et al. and Shin system in order to improve the viewing characteristics of LCD (See Col. 2, Lines 38-40 in Kim et al. reference).

As to claims 8-9, 11-12 Takahara et al. teaches to detect a timing for transmitting a display datum to be transmitted to the output terminal being not connected to the drain lines (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4) and Shin teaches to transmit a display datum being read out from either of the first and second storing means as the display datum to be transmitted to the output terminal not being connected to the drain lines (See Figs. 7-8, items 230a-230b, 240, 250, from Col. 5, line 54 to Col. 6, line 17).

As to claims 18-19, Shin teaches display control device transmits datum to the output control terminal through driving circuits display datum (See Figs. 7-8, items 230a-230b, 240, 250, from Col. 5, line 54 to Col. 6, line 17).

Shin does not teach the display control device transmits to output terminal being not connected to the drain, signal lines display datum being transmitted prior or subsequently to an output terminal being connected to one of the drain signal lines.

Takahara et al. teaches at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines (See Drawing 2, item 25) and to skip unconnected pins by generating start pulses for each IC with clock pulses (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4).

It would have been obvious to one of ordinary skill in the art at the time of invention to use start and clock pulses as shown by Takahara et al. as input to Shin display control device to transmit to output terminal being not connected to the drain lines a display datum having a same level as that of display datum being transmitted prior or subsequently to an output terminal being connected to one of the drain signal lines in order to use the same driving circuit for a LCD panel when the output bit number of a driver IC is larger than the circuit number of the divided electrode groups (See from page 2, last line to page 3, line 3 in Takahara et al).

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Takahara et al., Kim et al. and Liu et al. (US Patent No. 5,124,590).

As to claim 1, Shin teaches a liquid crystal display device, comprising: a liquid crystal display element with plurality of drain signal (data) lines (See Fig. 2, items 15, 24, Col. 1, Lines 36-45), a plurality of driving circuits including a first driving circuit and a second driving circuit, each of the driving circuits having a plurality of output terminals (See Fig 7, items 240, 250, 270, 280, 290, Col. 5, Lines 28-53); a display control device transmitting display data alternately to one of the output terminals of the first driving circuit and to one of the output terminals of the second driving circuit which is arranged next to the first driving circuit (See Fig. 7, items 200, 220, Col. 5, Lines 28-53).

Shin does not teach at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines and each of the remaining output terminal being connected to one of the drain signal lines.

Takahara et al. teaches at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines (See Drawing 2, item 25) and to skip unconnected pins by generating start pulses for each IC with clock pulses (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Takahara et al. into Shin system in order to use the same driving circuit for a LCD panel when the output bit number of a driver IC is larger than the circuit number of the divided electrode groups (See from page 2, last line to page 3, line 3 in Takahara et al).

Shin and Takahara et al. do not teach the display control device transmits to output terminal being not connected to the drain signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines.

Kim et al. teaches the display control device transmits to output terminal signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines (See Fig. 5, items Vi, Ui, Col.5, Lines 26-39).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Kim et al. into Takahara et al. and Shin system in order to improve the viewing characteristics of LCD (See Col. 2, Lines 38-40 in Kim et al. reference).

Kim et al., Takahara et al. and Shin do not disclose identical voltage for connected and unconnected pins.

Liu et al. teaches identical voltage for connected and unconnected pins (See Fig. 3, item VDD/2, Col. 5, Lines 50-53).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Liu et al. into Kim et al., Takahara et al. and Shin system in order to provide unconnected (floating) pins (See Col.1, Lines 43-45 in Liu et al. reference).

As to claim 2, improve the Shin teaches a display device, comprising: a display element with plurality of drain signal (data) lines (See Figs. 2, 7, items 15, 24, Col. 1,

Lines 36-45), a plurality of driving circuits including a first driving circuit and a second driving circuit, each of the driving circuits having a plurality of output terminals (See Fig 7, items 240, 250, 270, 280, 290, Col. 5, Lines 28-53); a display control device transmitting display data alternately to one of the output terminals of the first driving circuit and to one of the output terminals of the second driving circuit which is arranged next to the first driving circuit (See Fig. 7, items 200, 220, Col. 5, Lines 28-53).

Shin does not teach at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines and each of the remaining output terminal being connected to one of the drain signal lines.

Takahara et al. teaches at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines (See Drawing 2, item 25) and to skip unconnected pins by generating start pulses for each IC with clock pulses (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Takahara et al. into Shin system in order to use the same driving circuit for a LCD panel when the output bit number of a driver IC is larger than the circuit number of the divided electrode groups (See from page 2, last line to page 3, line 3 in Takahara et al).

Shin and Takahara et al. do not teach the display control device transmits to output terminal being not connected to the drain signal lines a display datum being

transmitted prior or subsequently to an output terminal being connected to one of drain signal lines.

Kim et al. teaches the display control device transmits to output terminal signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines (See Fig. 5, items Vi, Ui, Col.5, Lines 26-39).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Kim et al. into Takahara et al. and Shin system in order to improve the viewing characteristics of LCD (See Col. 2, Lines 38-40 in Kim et al. reference).

Kim et al., Takahara et al. and Shin do not disclose identical voltage for connected and unconnected pins.

Liu et al. teaches identical voltage for connected and unconnected pins (See Fig. 3, item VDD/2, Col. 5, Lines 50-53).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Liu et al. into Kim et al., Takahara et al. and Shin system in order to provide unconnected (floating) pins (See Col.1, Lines 43-45 in Liu et al. reference).

As to claim 3, Shin teaches a liquid crystal display device, comprising: a liquid crystal display element with plurality of drain signal (data) lines (See Figs. 2, 7, items 15, 24, Col. 1, Lines 36-45), a plurality of driving circuits including at least one odd numbered driving circuit and at least one even numbered driving circuit, each of the

driving circuits having a plurality of output terminals (See Fig 7, items 240, 250, 270, 280, 290, Col. 5, Lines 28-53); a display control device transmitting display data alternately to one of the output terminals of even driving circuit and to one of the output terminals of the second driving circuit which is arranged next to odd driving circuit (See Fig. 7, items 200, 220, Col. 5, Lines 28-53).

Shin does not teach at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines and each of the remaining output terminal being connected to one of the drain signal lines.

Takahara et al. teaches at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines (See Drawing 2, item 25) and to skip unconnected pins by generating start pulses for each IC with clock pulses (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Takahara et al. into Shin system in order to use the same driving circuit for a LCD panel when the output bit number of a driver IC is larger than the circuit number of the divided electrode groups (See from page 2, last line to page 3, line 3 in Takahara et al).

Shin and Takahara et al. do not teach the display control device transmits to output terminal being not connected to the drain signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines.

Kim et al. teaches the display control device transmits to output terminal signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines (See Fig. 5, items Vi, Ui, Col.5, Lines 26-39).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Kim et al. into Takahara et al. and Shin system in order to improve the viewing characteristics of LCD (See Col. 2, Lines 38-40 in Kim et al. reference).

Kim et al., Takahara et al. and Shin do not disclose identical voltage for connected and unconnected pins.

Liu et al. teaches identical voltage for connected and unconnected pins (See Fig. 3, item VDD/2, Col. 5, Lines 50-53).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Liu et al. into Kim et al., Takahara et al. and Shin system in order to provide unconnected (floating) pins (See Col.1, Lines 43-45 in Liu et al. reference).

As to claim 4, Shin teaches a display device, comprising: a display element with plurality of drain signal (data) lines (See Figs. 2, 7, items 15, 24, Col. 1, Lines 36-45), a plurality of driving circuits including at least one odd numbered driving circuit and at least one even numbered driving circuit, each of the driving circuits having a plurality of output terminals (See Fig 7, items 240, 250, 270, 280, 290, Col. 5, Lines 28-53); a display control device transmitting display data alternately to one of the output terminals

of odd numbered driving circuit and to one of the output terminals of even numbered driving circuit which is arranged next to the first driving circuit (See Fig. 7, items 200, 220, Col. 5, Lines 28-53).

Shin does not teach at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines and each of the remaining output terminal being connected to one of the drain signal lines.

Takahara et al. teaches at least one of first and second driving circuits has at least one output terminal not being connected to the drain signal lines (See Drawing 2, item 25) and to skip unconnected pins by generating start pulses for each IC with clock pulses (See Drawings 2-3, items 24-25, ST1, ST2, ..., from page 9, Line 3 to page 10, Line 4).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Takahara et al. into Shin system in order to use the same driving circuit for a LCD panel when the output bit number of a driver IC is larger than the circuit number of the divided electrode groups (See from page 2, last line to page 3, line 3 in Takahara et al).

Shin and Takahara et al. do not teach the display control device transmits to output terminal being not connected to the drain signal lines a display datum being transmitted prior or subsequently to an output terminal being connected to one of drain signal lines.

Kim et al. teaches the display control device transmits to output terminal signal lines a display datum being transmitted prior or subsequently to an output terminal

being connected to one of drain signal lines (See Fig. 5, items Vi, Ui, Col.5, Lines 26-39).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Kim et al. into Takahara et al. and Shin system in order to improve the viewing characteristics of LCD (See Col. 2, Lines 38-40 in Kim et al. reference).

Kim et al., Takahara et al. and Shin do not disclose identical voltage for connected and unconnected pins.

Liu et al. teaches identical voltage for connected and unconnected pins (See Fig. 3, item VDD/2, Col. 5, Lines 50-53).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Liu et al. into Kim et al., Takahara et al. and Shin system in order to provide unconnected (floating) pins (See Col.1, Lines 43-45 in Liu et al. reference).

Response to Arguments

3. Applicant's arguments filed on 08-11-05 with respect to claims 7-12, 18-19 have been fully considered but they are not persuasive:

On page 12, last paragraph Applicant's stated that Kim does not show the identical **voltage** datum for independent claims 7, 10. However, that independent claims 7, 10 do not recite limitation as **voltage** datum, only display datum as already

rejected by combination of Shin, Takahara and Kim (See Kim's "the same gray level" in Col. 5, Lines 37-40).

Notice, that limitation "an identical voltage" was added onlyto independent claims 1-4.

4. Applicant's arguments filed on 08-11-05 with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
11.03.05

AMR A. AWAD
PRIMARY EXAMINER

Replacement sheet

O.K.
to enter
L.S. 11.03.05

FIG. 6A

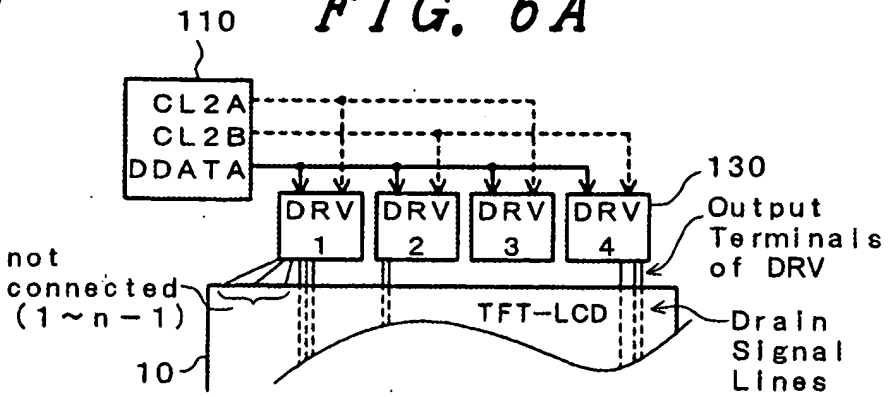

FIG. 6B

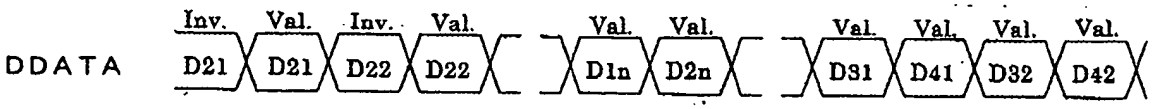

FIG. 6C

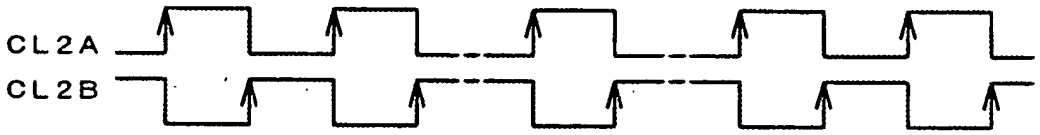

FIG. 7